

# PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD/13/7945 Dated 18 Jun 2013

Capacity expansion, for the product housed in TO-220 package at the Nantong Fujitsu Microelectronics (China) Subcontractor plant

#### Table 1. Change Implementation Schedule

| Forecasted implementation date for change   | 10-Sep-2013 |
|---|-------------|
| Forecasted availability date of samples for customer  | 11-Jun-2013 |
| Forecasted date for <b>STMicroelectronics</b><br>change Qualification Plan results availability | 11-Jun-2013 |
| Estimated date of changed product first shipment  | 17-Sep-2013 |

#### Table 2. Change Identification

| Product Identification<br>(Product Family/Commercial Product) | see attached list  |
|---|--|
| Type of change  | Assembly additional location   |
| Reason for change   | To improve service to ST Customers   |
| Description of the change                                     | To respond the ever increasing demand for the products housed in<br>TO-220 package, ST is glad to announce the expansion of capacity at<br>Nantong Fujitsu Microelectronics (China) Subcontractor factory, For<br>the complete list of the part numbers affected by this change, please<br>refer to the attached Products List |
| Change Product Identification                                 | will be ensured by the first two digits of the traceability code ("GF")  |
| Manufacturing Location(s)                                     |  |

#### Table 3. List of Attachments

| Customer Part numbers list |  |
|----------------------------|--|
| Qualification Plan results |  |

|   | >\$               |
|---|-------------------|
| Customer Acknowledgement of Receipt                       | PCN IPD/13/7945   |
| Please sign and return to STMicroelectronics Sales Office | Dated 18 Jun 2013 |
| Qualification Plan Denied                                 | Name:             |
| Qualification Plan Approved                               | Title:            |
|   | Company:          |
| Change Denied   | Date:             |
| Change Approved   | Signature:        |
| Remark  |                   |
|   |                   |
|   |                   |
|   |                   |
|   |                   |
|   |                   |
|   |                   |
|   |                   |
|   |                   |

| Name                | Function          |
|---------------------|-------------------|
| Giuffrida, Antonino | Marketing Manager |
| Martelli, Nunzio    | Product Manager   |
| Vitali, Gian Luigi  | Q.A. Manager      |

### **DOCUMENT APPROVAL**



# **IPD** Group

Assembly and Testing capacity expansion, for the product housed in TO-220 package, at the Nantong Fujitsu Microelectronics (China) Subcontractor plant.

Packages typology



#### WHAT:

To respond the ever increasing demand for the products housed in TO-220 package, ST is glad to announce the expansion of capacity at Nantong Fujitsu Microelectronics (China) Subcontractor factory,

For the complete list of the part numbers affected by this change, please refer to the attached Products List

**Samples**, are available right now upon request for immediate customer qualification, while the full availability of products will be granted from wk 22 2013 onwards,

#### WHY:

• To improve service to ST Customers

#### HOW:

By expanding capacity according the ST quality and reliability standard.

The changed here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant product's datasheets. There are as well no modifications in the packing modes nor in the standard delivery quantities either it may affect ST's Customers assembly methods.

#### **Qualification program and results:**

The qualification program consists mainly of comparative electrical characterization and reliability tests.Please refer to Appendix 1 for all the details.

#### WHEN:

Production start and first shipments will occur as indicated in the table below.

| Affected Product Types | Samples | 1 <sup>st</sup> Shipment |
|------------------------|---------|--------------------------|
| PowerMOSFET            | Now     | Wk22                     |
| Power Bipolar          | Now     | Wk22                     |
| Thyristor & Triac      | Now     | Wk22                     |
| Rectifier              | Now     | Wk22                     |

# Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled in the Nantong Fujitsu Microelectronics Subcontractor factory, will be ensured by the first two digits of the traceability code ("GF").

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.



# **Reliability Report**

Assembly and Testing capacity expansion, for the product housed in TO-220 package, at the NFME (China)Subcontractor plant.

| General Information     |  | Locations                  |   |
|-------------------------|--|----------------------------|---|
| Product Lines:          | ED7K / EZ66                            | Wafer Diffusion<br>Plants: | ED7K: Global Foundries<br>EZ66: AngMoKio<br>(SINGAPORE) |
| Product Families:       | Power MOSFET                           |                            |   |
| P/Ns:                   | STP140NF75 (ED7K)<br>STP10NK60Z (EZ66) | EWS Plants:                | ED7K: Global Foundries<br>EZ66: AngMoKio<br>(SINGAPORE) |
| Product Group:          | IMS - IPD                              | Assembly plant:            | NFME CHINA  |
| Product division:       | Power Transistor Division              | Reliability Lab:           | IMS-IPD Catania Reliability                             |
| Package:                | TO-220                                 |                            | Lab.  |
| Silicon Process techn.: | PowerMOSFET - StripFET™                |                            |   |

#### **DOCUMENT INFORMATION**

| Version | Date     | Pages | Prepared by | Approved by | Comment     |
|---------|----------|-------|-------------|-------------|-------------|
| 1.0     | May 2013 | 8     | C. Cappello | G.Falcone   | First issue |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.



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# **1** APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description                                       |  |
|--------------------|---|--|
| JESD47             | Stress-Test-Driven Qualification of Integrated Circuits |  |
|                    |   |  |

### 2 GLOSSARY

| DUT | Device Under Test |  |
|-----|-------------------|--|
| SS  | Sample Size       |  |
| HF  | Halogen Free      |  |

# **<u>3 RELIABILITY EVALUATION OVERVIEW</u>**

#### 3.1 **Objectives**

Qualification of the TO-220 package graded Molding Compound manufactured in the NFME (China) Subcontractor assy plant.

### 3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.



# **<u>4</u> DEVICE CHARACTERISTICS**

### 4.1 **Device description**

N-channel Power MOSFET

# 4.2 Construction note

### D.U.T.: STP140NF75 LINE: ED7K PACKAGE: TO-220

| Wafer/Die fab. information       |                              |  |
|----------------------------------|------------------------------|--|
| Wafer fab manufacturing location | Global Foundries (Singapore) |  |
| Technology                       | Power MOSFET - StripFET™     |  |
| Die finishing back side          | Ti/Ni/Ag                     |  |
| Die size                         | 4610 x 6350 μm <sup>2</sup>  |  |
| Metal                            | Al/Si/Cu                     |  |
| Passivation type                 | None                         |  |

| Wafer Testing (EWS) information           |                              |  |  |  |  |
|---|------------------------------|--|--|--|--|
| Electrical testing manufacturing location | Global Foundries (Singapore) |  |  |  |  |
| Test program                              | WPIS                         |  |  |  |  |

| Assembly information                |                   |  |  |  |
|-------------------------------------|-------------------|--|--|--|
| Assembly site                       | NFME (China)      |  |  |  |
| Package description                 | TO-220            |  |  |  |
| Molding compound                    | HF Epoxy Resin    |  |  |  |
| Frame material                      | Copper            |  |  |  |
| Die attach process                  | Soft Solder       |  |  |  |
| Die attach material                 | Pb/Ag/Sn          |  |  |  |
| Wire bonding process                | Ultrasonic        |  |  |  |
| Wires bonding materials             | AI 5 mils Gate    |  |  |  |
| -                                   | AI 15 mils Source |  |  |  |
| Lead finishing/bump solder material | Pure Tin          |  |  |  |

| Final testing information     |  |  |  |
|-------------------------------|--|--|--|
| Testing location NFME (China) |  |  |  |
| Tester TESEC                  |  |  |  |



### D.U.T.: STP10NK60Z LINE: EZ66 PACKAGE: TO-220

| Wafer/Die fab. information       |                             |  |  |  |
|----------------------------------|-----------------------------|--|--|--|
| Wafer fab manufacturing location | AngMoKio (Singapore)        |  |  |  |
| Technology                       | Power MOSFET - StripFET™    |  |  |  |
| Die finishing back side          | Ti/Ni/Au                    |  |  |  |
| Die size                         | 4950 x 3810 μm <sup>2</sup> |  |  |  |
| Metal                            | Al/Si                       |  |  |  |
| Passivation type                 | Nitride                     |  |  |  |

| Wafer Testing (EWS) information                                |      |  |  |  |  |
|--|------|--|--|--|--|
| Electrical testing manufacturing location AngMoKio (Singapore) |      |  |  |  |  |
| Test program   | WPIS |  |  |  |  |

| Assembly information                |                   |  |  |  |
|-------------------------------------|-------------------|--|--|--|
| Assembly site                       | NFME (China)      |  |  |  |
| Package description                 | TO-220            |  |  |  |
| Molding compound                    | HF Epoxy Resin    |  |  |  |
| Frame material                      | Copper            |  |  |  |
| Die attach process                  | Soft Solder       |  |  |  |
| Die attach material                 | Pb/Ag/Sn          |  |  |  |
| Wire bonding process                | Ultrasonic        |  |  |  |
| Wires bonding materials             | Al 5 mils Gate    |  |  |  |
|                                     | AI 10 mils Source |  |  |  |
| Lead finishing/bump solder material | Pure Tin          |  |  |  |

| Final testing information     |  |  |  |
|-------------------------------|--|--|--|
| Testing location NFME (China) |  |  |  |
| Tester TESEC                  |  |  |  |



# 5 TESTS RESULTS SUMMARY

#### 5.1 Test vehicle

| Lot # | Process/ Package  | Product Line | Comments     |
|-------|-------------------|--------------|--------------|
| 1     | STP140NF75        | ED7K         | Power MOSFET |
| 2     | 2 STP10NK60Z EZ66 |              | Power MOSFET |

## 5.2 Reliability test plan summary

# Lot. 1 - D.U.T.: STP140NF75 LINE: ED7K PACKAGE: TO-220

| Test  | PC                                    | Ctal not                    | Conditions                          | 66 | Ctomo           | Failure/SS |
|-------|---------------------------------------|-----------------------------|-------------------------------------|----|-----------------|------------|
| Test  | PC                                    | Std ref.                    | Conditions                          | SS | Steps           | Lot 1      |
|       |                                       | JESD22                      |                                     |    | 168 H           |            |
| HTRB  | Ν                                     | A-108                       | T.A.=175°C Vdss=60V                 | 77 | 500 H           | 0/77       |
|       |                                       | A-100                       |                                     |    | 1000 H          |            |
|       |                                       | JESD22                      |                                     |    | 168 H           |            |
| HTGB  | Ν                                     | A-108                       | TA = 150°C Vgss= 20V                | 77 | 500 H           | 0/77       |
|       |                                       | 77100                       |                                     |    | 1000 H          |            |
|       |                                       | JESD22                      | TA = 175°C                          | 77 | 168 H           | 0/77       |
| HTSL  | Ν                                     | A-103                       |                                     |    | 500 H           |            |
|       |                                       | 7, 100                      |                                     |    | 1000 H          |            |
|       |                                       | N JESD22<br>A-101           | Ta=85°C Rh=85%,<br>Vdss=50V         | 77 | 168 H           | 0/77       |
| H3TRB | Ν                                     |                             |                                     |    | 500 H           |            |
|       |                                       | 77101                       | 1000-001                            |    | 1000 H          |            |
|       |                                       | N JESD22<br>A-104           | TA=-65°C TO 150°C<br>(1 HOUR/CYCLE) | 77 | 100 cy          |            |
| TC    | Ν                                     |                             |                                     |    | 200 cy          | 0/77       |
|       | · · · · · · · · · · · · · · · · · · · |                             | (                                   |    | 500 cy          |            |
| AC    | Ν                                     | JESD22<br>A-102             | TA=121°C – PA=2 ATM                 | 77 | 96 H            | 0/77       |
| TF    | Ν                                     | Mil-Std 750D<br>Method 1037 | ∆Tc=105°C                           | 77 | 5 Kcy<br>10 Kcy | 0/77       |



# Lot. 2 - D.U.T.: STP10NK60Z LINE: EZ66 PACKAGE: TO-220

| Test  | PC | Std ref.                    | Conditions                          | SS | Steps           | Failure/SS<br>Lot 2 |
|-------|----|-----------------------------|-------------------------------------|----|-----------------|---------------------|
|       |    | JESD22                      |                                     |    | 168 H           |                     |
| HTRB  | Ν  | A-108                       | T.A.=150°C Vdss=480V                | 77 | 500 H           | 0/77                |
|       |    | A-100                       |                                     |    | 1000 H          |                     |
|       |    | JESD22                      |                                     |    | 168 H           |                     |
| HTGB  | Ν  | A-108                       | TA = 150°C Vgss= 30V                | 77 | 500 H           | 0/77                |
|       |    | A-100                       |                                     |    | 1000 H          |                     |
|       |    | JESD22                      | TA = 150°C                          | 77 | 168 H           |                     |
| HTSL  | Ν  | A-103                       |                                     |    | 500 H           | 0/77                |
|       |    | A-105                       |                                     |    | 1000 H          |                     |
|       |    | N JESD22<br>A-101           | Ta=85°C Rh=85%,<br>Vdss=100V        | 77 | 168 H           | 0/77                |
| H3TRB | Ν  |                             |                                     |    | 500 H           |                     |
|       |    |                             |                                     |    | 1000 H          |                     |
|       |    | N JESD22<br>A-104           | TA=-65°C TO 150°C<br>(1 HOUR/CYCLE) | 77 | 100 cy          |                     |
| TC    | Ν  |                             |                                     |    | 200 cy          | 0/77                |
|       |    |                             | (                                   |    | 500 cy          |                     |
| AC    | Ν  | JESD22<br>A-102             | TA=121°C – PA=2 ATM                 | 77 | 96 H            | 0/77                |
| TF    | Ν  | Mil-Std 750D<br>Method 1037 | ∆Tc=105°C                           | 77 | 5 Kcy<br>10 Kcy | 0/77                |



# <u>6</u> <u>ANNEXES 6.0</u>

## **6.1Tests Description**

| Test name  | Description  | Purpose  |  |
|--|--|--|--|
| HTRB<br>High Temperature<br>Reverse Bias                               | The device is stressed in static configuration,<br>trying to satisfy as much as possible the<br>following conditions:  | To determine the effects of bias conditions and<br>temperature on solid state devices over time. It<br>simulates the devices' operating condition in an<br>accelerated way.  |  |
| <b>HTGB</b><br>High Temperature<br>Forward (Gate)<br>Bias              | <ul> <li>low power dissipation;</li> <li>max. supply voltage compatible with diffusion process and internal circuitry limitations;</li> </ul>                                      | To maximize the electrical field across either<br>reverse-biased junctions or dielectric layers, in<br>order to investigate the failure modes linked to<br>mobile contamination, oxide ageing, layout<br>sensitivity to surface effects.   |  |
| HTSL<br>High Temperature<br>Storage Life                               | The device is stored in unbiased condition at<br>the max. temperature allowed by the<br>package materials, sometimes higher than<br>the max. operative temperature.                | To investigate the failure mechanisms activated<br>by high temperature, typically wire-bonds solder<br>joint ageing, data retention faults, metal stress-<br>voiding.  |  |
| AC<br>Auto Clave<br>(Pressure Pot)                                     | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.   | To investigate corrosion phenomena affecting<br>die or package materials, related to chemical<br>contamination and package hermeticity.  |  |
| TC<br>Temperature<br>Cycling   | The device is submitted to cycled<br>temperature excursions, between a hot and a<br>cold chamber in air atmosphere.  | To investigate failure modes related to the<br>thermo-mechanical stress induced by the<br>different thermal expansion of the materials<br>interacting in the die-package system. Typical<br>failure modes are linked to metal displacement,<br>dielectric cracking, molding compound<br>delamination, wire-bonds failure, die-attach<br>layer degradation. |  |
| H3TRB<br>Temperature<br>Humidity Bias                                  | The device is biased in static configuration<br>minimizing its internal power dissipation, and<br>stored at controlled conditions of ambient<br>temperature and relative humidity. | To evaluate the package moisture resistance<br>with electrical field applied, both electrolytic and<br>galvanic corrosion are put in evidence.   |  |
| <b>TF / IOL</b><br>Thermal Fatigue /<br>Intermittent<br>Operating Life | The device is submitted to cycled<br>temperature excursions generated by power<br>cycles (ON/OFF) at T ambient.  | To investigate failure modes related to the<br>thermo-mechanical stress induced by the<br>different thermal expansion of the materials<br>interacting in the die-package system. Typical<br>failure modes are linked to metal displacement,<br>dielectric cracking, molding compound<br>delamination, wire-bonds failure, die-attach<br>layer degradation. |  |



# Qualification of Rectifiers in TO-220AB package: Additional Assembly and Test Location in China

| General             | Information  | Locations       |                                     |  |
|---------------------|--|-----------------|-------------------------------------|--|
| Product Line        | Rectifiers (BU78)  | Wafer fab       | STM Singapore<br>STM Tours (France) |  |
| Product Description | Bipolar, Turboswitch and<br>Power Schottky in TO-220AB<br>package: Additional<br>assembly and test location in | Assembly plant  | Subcontractor (China)               |  |
|                     | China  | Reliability Lab | STM Tours (France)                  |  |
| Product Group       | IPD  |                 |                                     |  |
| Product division    | ASD & IPAD   |                 |                                     |  |
| Package             | TO-220AB (3 leads)   |                 |                                     |  |
| Maturity level step | Qualified  |                 |                                     |  |

#### **DOCUMENT INFORMATION**

| Version | Date        | Pages | Prepared by | Comment   |
|---------|-------------|-------|-------------|---|
| 1.0     | 18-Feb-2013 | 9     | I. BALLON   | First issue<br>Qualification of Rectifiers (Bipolar, Turboswitch and<br>Power Schottky in TO-220AB package: Additional<br>assembly and test location in China |

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks

during the product life using a set of defined test methods. This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.



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# **<u>1</u>** APPLICABLE AND REFERENCE DOCUMENTS

| Document reference | Short description                                       |
|--------------------|---|
| JESD47             | Stress-Test-Driven Qualification of Integrated Circuits |
| SOP 2614           | Reliability requirements for product qualification      |
| 0061692            | Reliability tests and criteria for qualifications       |
| FMEA               | 8419012   |
| RER                | 1242001   |

# 2 GLOSSARY

| DUT  | Device Under Test             |
|------|-------------------------------|
| PCB  | Printed Circuit Board         |
| SS   | Sample Size                   |
| HTRB | High Temperature Reverse Bias |
| TC   | Temperature Cycling           |
| PCT  | Pressure Pot 2 bars           |
| THB  | Temperature Humidity Bias     |
| IOLT | Intermittent Operational Life |
| RSH  | Resistance to Solder Heat     |
| SD   | Solderability                 |

### 3 RELIABILITY EVALUATION OVERVIEW

#### 3.1 **Objectives**

The objective of this report is to qualify new subcontractor for TO-220AB (3 leads) package for Rectifiers devices

The product series currently involved in this qualification are listed below.

| Product sub-Family | Commercial product |
|--------------------|--------------------|
| Rectifiers         | STPSxxxCT          |
| Rectifiers         | STTHxxxCT          |

Specific devices not expressly listed in the above table are included in this change.

The reliability methodology used follows the JESD47-E: « Stress Test Driven Qualification Methodology ». The following reliability tests ensuing are:

- HTRB to evaluate the risk of contamination.
- THB to verify there is no apparition of corrosion and risk of moisture penetration.
- TC,RSH and IOLT to ensure the mechanical robustness of the products.
- Solderability to verify good wettability on leads

### 3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.



### **<u>4</u> DEVICE CHARACTERISTICS**

### 4.1 **Device description**

• Rectifiers (Bipolar, Turboswitch, Power Schottky) in TO-220AB (3 leads) package: Additional assembly and test location in China.

### 4.2 Construction note

|   | Rectifiers (STPSxxxCT-STTHxxxCT)<br>in TO-220AB package           |
|---|---|
| Wafer/Die fab. information                |   |
| Wafer fab manufacturing location          | STMicroelectronics Singapore<br>STMicroelectronics Tours (France) |
| Wafer Testing (EWS) information           |   |
| Electrical testing manufacturing location | STMicroelectronics Singapore<br>STMicroelectronics Tours (France) |
| Assembly information                      |   |
| Assembly site                             | Subcontractor (China)   |
| Package description                       | TO-220AB (3leads)   |
| Molding compound                          | Epoxy resin   |
| Lead finishing process                    | Electroplating  |
| Lead finishing material                   | Matte Tin (Sn 100%)   |
| Final testing information                 |   |
| Testing location                          | Subcontractor (China)   |

# 5 TESTS RESULTS SUMMARY

### 5.1 Test vehicles

| Lot # | Product       | Back End              | Package               | Product<br>Family |  |
|-------|---------------|-----------------------|-----------------------|-------------------|--|
| 1     | STTH16L06CT   |                       |                       | Turboswitch       |  |
| 2     | STTH2002CT    |                       |                       | Bipolar           |  |
| 3     | STPS40M100CT  | Subcontractor (China) | TO-220AB<br>(3 leads) |                   |  |
| 4     |               |                       | Power Schottky        |                   |  |
| 5     | STPS40SM100CT |                       |                       |                   |  |



# 5.2 Test plan and results summary

#### **Die Oriented Tests**

| Test PC Std ref. Conditions |    | Conditions        | SS Steps                  | Failure/SS |        |      | Note     |          |       |       |  |  |      |
|-----------------------------|----|-------------------|---------------------------|------------|--------|------|----------|----------|-------|-------|--|--|------|
| Test                        | FC | Stu lei.          | Conditions                | 33         | 33     | 33   | SS Steps | 33 Steps | Lot 1 | Lot 2 |  |  | Note |
| HTRB                        | Ν  | V JESD22<br>A-108 | $1 \sqrt{r} = (18)/(rrm)$ | 154        | 168 H  | 0/77 | 0/77     |          |       |       |  |  |      |
|                             |    |                   |                           |            | 500 H  | 0/77 | 0/77     |          |       |       |  |  |      |
|                             |    | A-106             |                           |            | 1000 H | 0/77 | 0/77     |          |       |       |  |  |      |

#### Package Oriented Tests

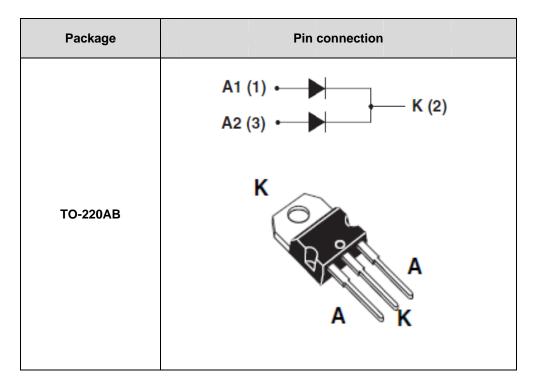
| Teet |    | Ctal rof                         | Conditions                                  | 66 | Stone                |       |       | Failu | re/SS | Nata     |
|------|----|----------------------------------|---|----|----------------------|-------|-------|-------|-------|----------|
| Test | PC | Std ref.                         | Conditions                                  | SS | Steps                | Lot 3 |       |       |       | Note     |
|      |    |                                  |   |    | 168 H                | 0/25  |       |       |       |          |
| THB  | Ν  | JESD22<br>A-101                  | Ta = 85°C, RH = 85%,<br>Vr = 0.8xVrrm       | 25 | 500 H                | 0/25  |       |       |       |          |
|      |    |                                  | or 100V max                                 |    | 1000 H               | 0/25  |       |       |       |          |
|      |    |                                  |   | SS | Steps                |       |       | Failu | re/SS | Note     |
|      |    |                                  |   | 33 | Sieps                | Lot 3 | Lot 5 |       |       | Note     |
|      |    | JESD22                           | Ta = -65°C to 150°C                         |    | 100 cy               | 0/25  | 0/25  |       |       |          |
| TC   | Ν  | A-104                            | 2 cycles/hour                               | 50 | 500 cy               | 0/25  | 0/25  |       |       |          |
|      |    |                                  |   | SS | Stone                |       |       | Failu | re/SS | <br>Nata |
|      |    |                                  |   | 22 | Steps                | Lot 2 |       |       |       | Note     |
| PCT  | Ν  | JESD22<br>A-102                  | 121°C, RH=100%,<br>P=2 bars                 | 77 | 96hrs                | 0/77  |       |       |       |          |
|      |    |                                  |   |    | 0                    |       |       | Failu | re/SS | Nete     |
|      |    |                                  |   | SS | Steps                | Lot 3 |       |       |       | Note     |
| IOLT | N  | MIL-STD<br>750<br>Method<br>1037 | Delta Tc=85°C,<br>Pon=3.5min<br>Poff=3.5min | 25 | 8572cy               | 0/25  |       |       |       |          |
|      |    |                                  |   |    |                      |       |       | Failu | re/SS | Note     |
|      |    |                                  |   |    |                      | Lot 5 |       |       |       | Note     |
| RSH  | Ν  | JESD22B-<br>106                  | 2 dipping at 260°C<br>10s On / 15s Off      | 12 |                      | 0/12  |       |       |       |          |
|      |    |                                  |   | SS | Steps                |       |       | Failu | re/SS | Note     |
|      |    |                                  |   | 33 | -                    | Lot 4 | Lot 5 |       |       | Note     |
|      |    |                                  | 245°C SnAgCu bath<br>Dry aging              | 20 | Visual<br>inspection | 0/10  | 0/10  |       |       |          |
|      |    |                                  | 245°C SnAgCu bath<br>Wet aging              | 20 | Visual<br>inspection | 0/10  | 0/10  |       |       |          |
| SD   | Ν  | J-STD-002                        |   |    |                      | Lot 4 | Lot 5 |       |       |          |
|      |    |                                  | 220°C SnPb bath Dry<br>aging                | 20 | Visual<br>inspection | 0/10  | 0/10  |       |       |          |
|      |    |                                  | 220°C SnPb bath Wet<br>aging                | 20 | Visual<br>inspection | 0/10  | 0/10  |       |       |          |



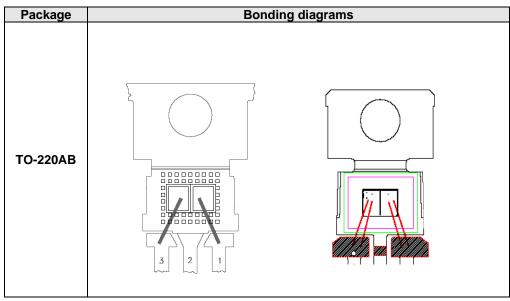
# 6 ANNEXES

# 6.1 **Device details**

#### 6.1.1 Pin connection



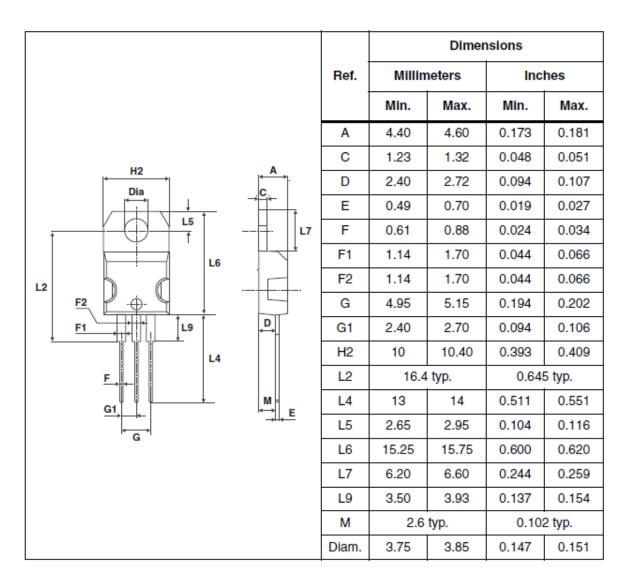
### 6.1.2 Bonding diagram





#### 6.1.3 Package outline/Mechanical data

• TO-220AB (3 leads)





# 6.2 **Tests description**

| Test name                                       | Description   | Purpose   |  |  |
|---|---|---|--|--|
| Die Oriented                                    |   |   |  |  |
| <b>HTRB</b><br>High Temperature<br>Reverse Bias | The device is stressed in static configuration,<br>trying to satisfy as much as possible the<br>following conditions:<br>low power dissipation;<br>max. supply voltage compatible with diffusion<br>process and internal circuitry limitations;           | To determine the effects of bias conditions and<br>temperature on solid state devices over time. It<br>simulates the devices' operating condition in an<br>accelerated way.<br>To maximize the electrical field across either<br>reverse-biased junctions or dielectric layers, in<br>order to investigate the failure modes linked to<br>mobile contamination, oxide ageing, layout<br>sensitivity to surface effects. |  |  |
| Package Oriented                                |   |   |  |  |
| TC<br>Temperature<br>Cycling                    | The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.   | To investigate failure modes related to the<br>thermo-mechanical stress induced by the<br>different thermal expansion of the materials<br>interacting in the die-package system. Typical<br>failure modes are linked to metal displacement,<br>dielectric cracking, molding compound<br>delamination, wire-bonds failure, die-attach<br>layer degradation.  |  |  |
| <b>THB</b><br>Temperature<br>Humidity Bias      | The device is biased in static configuration<br>minimizing its internal power dissipation, and<br>stored at controlled conditions of ambient<br>temperature and relative humidity.  | To evaluate the package moisture resistance<br>with electrical field applied, both electrolytic and<br>galvanic corrosion are put in evidence.  |  |  |
| PCT<br>Pressure Pot                             | The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.  | To investigate corrosion phenomena affecting<br>die or package materials, related to chemical<br>contamination and package hermeticity.   |  |  |
| IOLT  | case temperature (delta is the high minus the<br>low mounting surface temperatures) of<br>+85°C (+60°C for thyristors), followed by an<br>off period, when the power is suddenly<br>removed, for cooling the case through a<br>similar delta temperature. | The purpose of this test is to determine<br>compliance with the specified numbers of cycles<br>for devices subjected to the specified<br>conditions. It accelerates the stresses on all<br>bonds and interfaces between the chip and<br>mounting face of devices subjected to repeated<br>turn on and off of equipment and is therefore<br>most appropriate for case mount style (e.g.,                                 |  |  |



| Test name | Description  | Purpose  |
|-----------|--|--|
| RSH       |  | This test is used to determine whether solid<br>state devices can withstand the effects of the<br>temperature to which they will be subjected<br>during soldering of their leads. The heat is<br>conducted through the leads into the device<br>package from solder heat at the reverse side of<br>the board. This procedure does not simulate<br>wave soldering or reflow heat exposure on the<br>same side of the board as the package body. |
| SD        | The device is aged in a wet and dry bath of<br>solder. A preconditioning test is included in<br>this test method, which degrades the<br>termination finish to provide a guard band<br>against marginal finish. | To test whether the packaging materials and<br>processes used during the manufacturing<br>operations process produce a component that<br>can be successfully soldered to the next level<br>assembly using tin lead eutectic solder   |

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| STP3NK60Z   | STP3NK80Z   | STP3NK90Z  |
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| STP40NF10L  | STP40NF12   | STP40NF20  |
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| BD242C                            |  |
| STI76NF75                         |  |
| STPS10H100CT                      |  |
| BUL1203E                          |  |
|                                   |  |
| MQT-F                             |  |
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