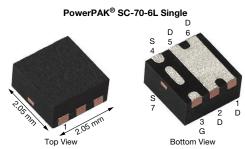




P-Channel 20 V (D-S) MOSFET



Marking code: BK

PRODUCT SUMMARY									
V _{DS} (V)	-20								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.025								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5 \text{ V}$	0.031								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8 \text{ V}$	0.041								
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.5 \text{ V}$	0.070								
Q _g typ. (nC)	24								
I _D (A) ^a	-12								
Configuration	Single								

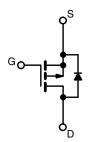
FEATURES

- TrenchFET® power MOSFET
- New thermally enhanced PowerPAK[®] SC-70 package
 - Small footprint area
 - Low on-resistance
- 100 % R_g tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



APPLICATIONS

 Load switch, PA switch and battery switch for portable devices



P-Channel MOSFET

ORDERING INFORMATION							
Package	PowerPAK SC-70						
Load (Dh) free and balagen free	SiA431DJ-T1-GE3						
Lead (Pb)-free and halogen-free	SiA431DJ-T4-GE3						

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	-20	V
Gate-source voltage		V _{GS}	V	
	T _C = 25 °C		-12 ^a	
Continuous drain surrent (T. 150 °C)	T _C = 70 °C	1 , [-12 ^a	
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	-9.6 ^{b, c}	
	T _A = 70 °C		-7.7 ^{b, c}	Α
Pulsed drain current		I _{DM}	-30	
Ocalia a casa sa data diada a casa	T _C = 25 °C		-12 ^a	
Continuous source-drain diode current	T _A = 25 °C	l _s	-2.9 ^{b, c}	
	T _C = 25 °C		19	
Maximum power dissipation	T _C = 70 °C		12	W
	T _A = 25 °C	P _D	3.5 ^{b, c}	VV
	T _A = 70 °C		2.2 b, c	
Operating junction and storage temperature rai	T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature	e) d, e		260	

THERMAL RESISTANCE RATINGS									
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT					
Maximum junction-to-ambient b, f	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.3	6.5]				

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 80 °C/W



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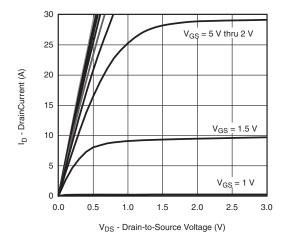
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT			
Static					L	l			
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20	-	-	V			
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$		-	-14.5	-				
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	2.7	-	mV/°C			
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-	-0.85	V			
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$	-	-	± 100	nA			
		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μΑ			
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10				
On-state drain current a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20	-	-	Α			
	B(OII)	$V_{GS} = -4.5 \text{ V}, I_D = -6.5 \text{ A}$	-	0.020	0.025	- 			
	_	V _{GS} = -2.5 V, I _D = -5.8 A	_	0.025	0.031	_			
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -1.8 V, I _D = -2.5 A	_	0.034	0.041	Ω			
		V _{GS} = -1.5 V, I _D = -1.5 A	_	0.045	0.070	\dashv			
Forward transconductance a	9 _{fs}	V _{DS} = -10 V, I _D = -6.5 A	-	31	-	S			
Dynamic ^b	, one			l	l.				
Input capacitance	C _{iss}		-	1700	-	pF			
Output capacitance	Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	230	-				
Reverse transfer capacitance	C _{rss}	, 45	-	205	-				
· 		V _{DS} = -10 V, V _{GS} = -8 V, I _D = -9.6 A	_	40	60	nC			
Total gate charge	Q _g		-	24	36				
Gate-source charge		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -9.6 \text{ A}$	_	2.4	-				
Gate-drain charge	Q _{qd}		-	6.5	-				
Gate resistance	Ra	f = 1 MHz	1.3	6.3	13	Ω			
Turn-on delay time	t _{d(on)}		-	22	35				
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_L = 1.3 \Omega,$	_	25	40				
Turn-off delay time	t _{d(off)}	$I_D \cong -7.7 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	_	65	100				
Fall time	t _f		_	25	40				
Turn-on delay time	t _{d(on)}		_	10	15	ns			
Rise time	t_r $V_{DD} = -10 \text{ V, R}_{I} = 1.3 \Omega,$		_	10	15	1			
Turn-off delay time	t _{d(off)}	$I_D \cong -7.7 \text{ A}, V_{GEN} = -8 \text{ V}, R_g = 1 \Omega$	_	65	100				
Fall time	t _f		_	20	30				
Drain-Source Body Diode Characterist				ı		ı			
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	-12				
Pulse diode forward current	I _{SM}	-	-	-	-30	A			
Body diode voltage	V _{SD}	I _S = -7.7 A, V _{GS} = 0 V	-	-0.8	-1.2	V			
Body diode reverse recovery time	t _{rr}	3 / 45	-	35	60	ns			
Body diode reverse recovery charge	Q _{rr}	$I_F = -7.7 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	-	21	35	nC			
Reverse recovery fall time	ta	$T_{J} = 25 ^{\circ}\text{C}$	-	20	-				
	-a	•			l	ns			

Notes

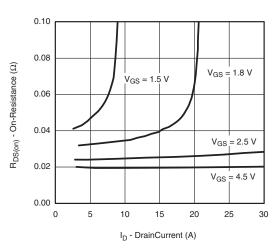
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

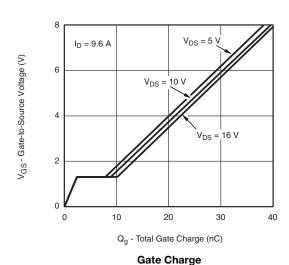


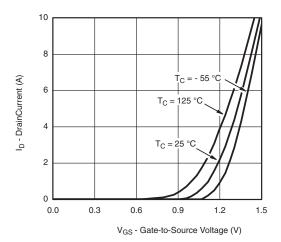


Output Characteristics

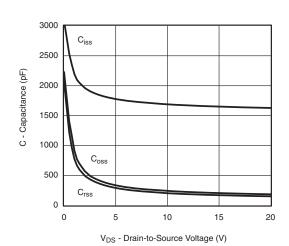


On-Resistance vs. Drain Current and Gate Voltage

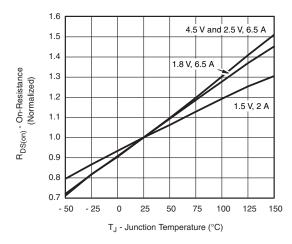




Transfer Characteristics

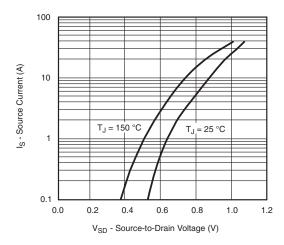


Capacitance

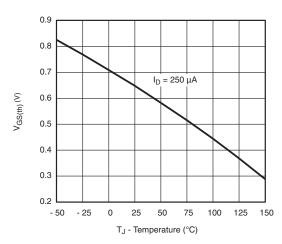


On-Resistance vs. Junction Temperature

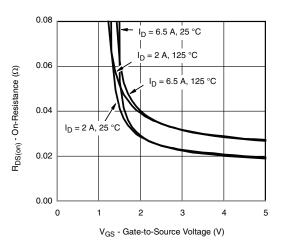




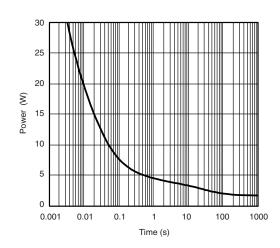
Source-Drain Diode Forward Voltage



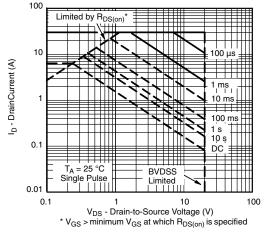
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

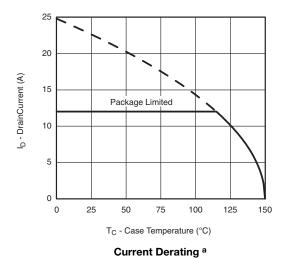


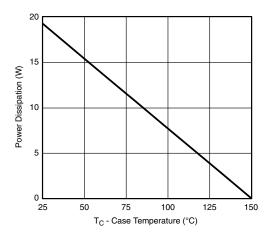
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient





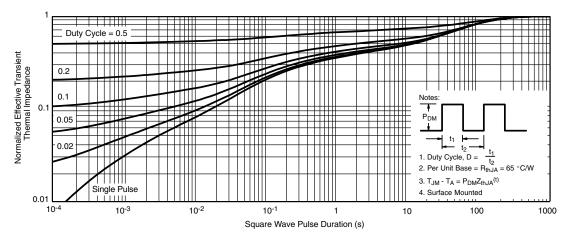


Power Derating

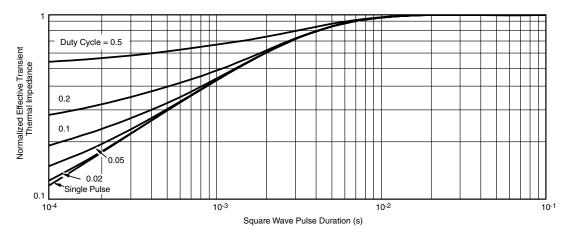
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

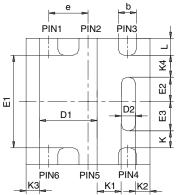
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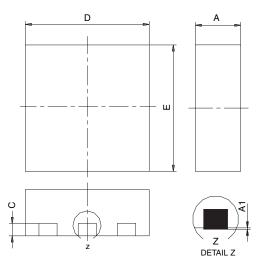
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP	1	0.275 TYP			0.011 TYP		
K1		0.400 TYP		0.016 TYP		0.320 TYP			0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP			0.010 TYP			
К3		0.225 TYP		0.009 TYP						•	•	
K4		0.355 TYP			0.014 TYP							
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

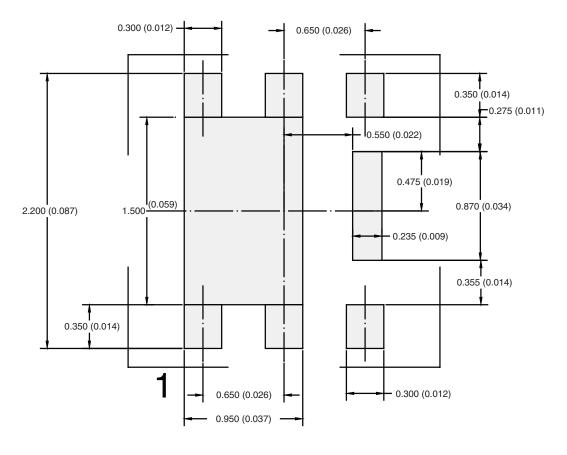
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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Vishay

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