8-Bit Shift and Store Register

High-Performance Silicon-Gate CMOS

The MC74HC4094A is a high speed CMOS 8—bit serial shift and storage register. This device consists of an 8—bit shift register and latch with 3—state output buffers. Data is shifted on positive clock (CP) transitions. The data in the shift register is transferred to the storage register when the Strobe (STR) input is high. The output buffers are enabled when the Output Enable (OE) input is set high. Two serial outputs (QS1, QS2) are available for cascading multiple devices.

Features

- Wide Operating Voltage Range: 2.0 to 6.0 V
- Low Power Dissipation: $I_{CC} = < 10 \mu A$
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Typical Applications

- Serial-to-Parallel Conversion
- Remote Control Storage Register



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MARKING DIAGRAMS

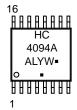


SOIC-16 D SUFFIX CASE 751B





TSSOP-16 DT SUFFIX CASE 948F



A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G, • = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

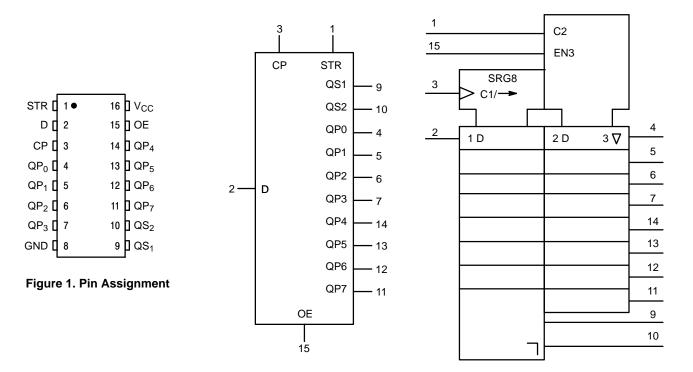


Figure 2. Logic Symbol

Figure 3. IEC Logic Symbol

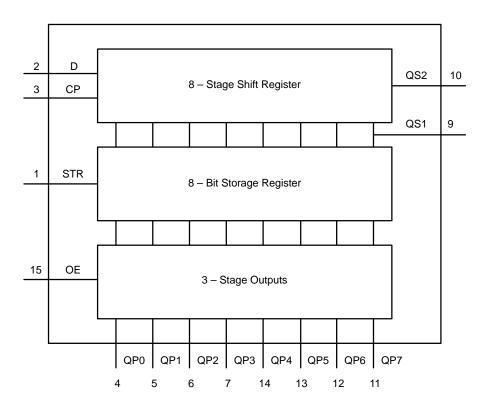


Figure 4. Functional Diagram

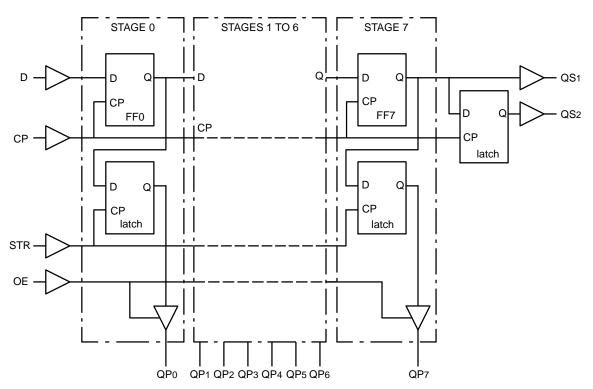


Figure 5. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating – SOIC Package: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{\rm CC}$). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to G	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package	- 55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

FUNCTIONAL TABLE

	INPUTS				PARALLEL OUTPUTS SERIAL (
СР	OE	STR	D	QP0	QPn	QS1	QS2
1	L	Х	Х	Z	Z	Q'6	NC
\downarrow	L	Х	Х	Z	Z	NC	QP7
1	Н	L	Х	NC	NC	Q'6	NC
1	Н	Н	L	L	QPn-1	Q'6	NC
1	Н	Н	Н	Н	QPn-1	Q'6	NC
\downarrow	Н	Н	Н	NC	NC	NC	QP7

Notes

- 1. H = HIGH voltage level
 - L = LOW voltage level
 - X = don't care
 - Z = high impedance OFF-state

 - NC = no change

 ↑ = LOW-to-HIGH CP transition

 ↓ = HIGH-to-LOW CP transition

 - Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

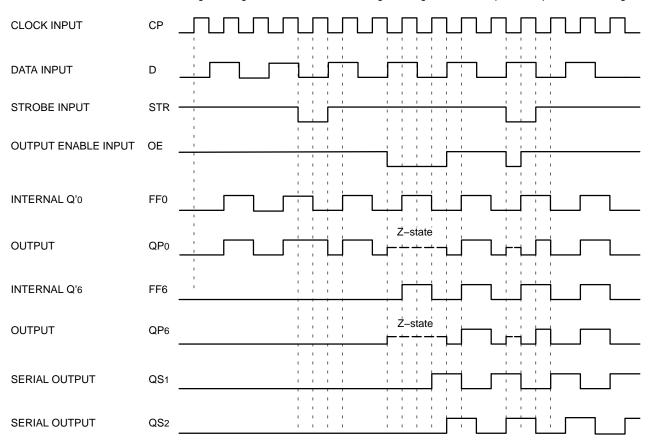


Figure 6. Timing Diagram

DC CHARACTERISTICS

				Guaranteed Limits			
Symbol	Parameter	Test Conditions	V _{CC} (V)	-55°C to 25°C	≤ 85°C	≤ 125°C	Uni
V_{IH}	Minimum High-Level Input	$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$	2.0	1.5	1.5	1.5	V
	Voltage	I _{OUT} ≤ 20 μA	3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input	$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$	2.0	0.5	0.5	0.5	V
	Voltage	I _{OUT} ≤ 20 μA	3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output	V _{IN} = V _{IH} or V _{IL}	2.0	1.9	1.9	1.9	V
	Voltage	I _{OUT} ≤ 20 μA	3.0	2.9	2.9	2.9	
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL} , $ _{OUT} = 2.4$ mA	3.0	2.75	2.7	2.6	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4 mA	4.5	4.25	4.2	4.1	
		$V_{IN} = V_{IH}$ or V_{IL} , $ _{OUT} = 5.2$ mA	6.0	5.75	5.7	5.6	
V _{OL}	Maximum Low-Level Output	$V_{IN} = V_{IH} \text{ or } V_{IL}, _{OUT} \le 20 \mu A$	2.0	0.1	0.1	0.1	V
	Voltage		3.0	0.1	0.1	0.1	
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL} , $ _{OUT} = 2.4$ mA	3.0	0.25	0.3	0.4	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4 mA	4.5	0.25	0.3	0.4	
		$V_{IN} = V_{IH}$ or V_{IL} , $ _{OUT} = 5.2$ mA	6.0	0.25	0.3	0.4	
I _{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	6.0	±0.1	±1	±1	μΑ
I _{OZ}	Maximum Tri-State Output Leakage Current	V _{IN} = V _{CC} or GND V _{OUT} = V _{CC} or GND	6.0	±0.5	±5	±10	μΑ
I _{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	6.0	4.0	40	80	μA

AC CHARACTERISTICS ($t_f = t_r = 6 \text{ ns}, C_L = 50 \text{ pF}$)

				Guaranteed Limits			
Symbol	Parameter	Test Conditions	V _{CC} (V)	-55°C to 25°C	≤ 85°C	≤ 125°C	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay	Figure 7	2.0	120	150	170	ns
	CP to QS ₁		3.0	90	100	110	
			4.5	30	38	45	
			6.0	26	33	38	
t _{PHL} , t _{PLH}	Maximum Propagation Delay	Figure 7	2.0	120	150	170	ns
	CP to QS ₂		3.0	90	100	110	
			4.5	27	34	41	
			6.0	23	29	35	
t _{PHL} , t _{PLH}	Maximum Propagation Delay	Figure 7	2.0	120	150	170	ns
	CP to QP _n		3.0	90	100	110	
			4.5	39	49	59	
			6.0	33	42	50	
t _{PHL} , t _{PLH}	Maximum Propagation Delay	Figure 8	2.0	120	150	170	ns
	STR to QP _n		3.0	90	100	110	
			4.5	36	45	54	
			6.0	31	38	46	
t _{PZH} , t _{PZL} Ma	Maximum 3-State Output Enable Time	Figure 9	2.0	120	140	160	ns
	OE to QP _n		3.0	80	100	120	
			4.5	35	44	53	
			6.0	30	37	45	
t _{PHZ} , t _{PLZ}	Maximum 3-State Output Enable Time	Figure 9	2.0	100	120	140	ns
	OE to QP _n		3.0	70	90	110	
			4.5	25	31	38	
			6.0	21	26	32	
t _{THL} , t _{TLH}	Maximum Output Transition Time	Figure 7	2.0	70	90	110	ns
			3.0	40	60	80	
			4.5	18	22	25	
			6.0	16	19	22	
t _W	Minimum Clock Pulse Width	Figure 7	2.0	80	100	120	ns
	High or Low		3.0	50	60	80	
			4.5	16	20	24	
			6.0	14	17	20	
t _W	Minimum Strobe Pulse Width	Figure 8	2.0	80	100	120	ns
	High		3.0	50	60	80	
			4.5	16	20	24	
			6.0	14	17	20	
t _{SU}	Minimum Set-up Time	Figure 10	2.0	50	65	75	ns
	D to CP		3.0	30	35	45	
			4.5	10	13	15	
			6.0	9	11	13	1

AC CHARACTERISTICS ($t_f = t_r = 6 \text{ ns}, C_L = 50 \text{ pF}$)

				Guar	ts			
Symbol	Parameter	Test Conditions	V _{CC} (V)	-55°C to 25°C	≤ 85°C	≤ 125°C	Unit	
t _{SU}	Minimum Set-up Time	Figure 8	2.0	100	125	150	ns	
	CP to STR		3.0	60	75	90	1	
			4.5	20	25	30	1	
			6.0	17	21	26	1	
t _h	Minimum Hold Time	Figure 10	2.0	3	3	3	ns	
	D to CP		3.0	3	3	3	1	
		†	4.5	3	3	3		
			6.0	3	3	3	1	
t _h	Minimum Hold Time	Figure 8	2.0	0	0	0	ns	
	CP to STR	OF 10 STK	CF IO STR	3.0	0	0	0	
			4.5	0	0	0		
			6.0	0	0	0		
f _{MAX}	Minimum Clock Pulse Frequency	Figure 7	2.0	6	5	4	MHz	
			3.0	18	14	12		
			4.5	30	24	20		
			6.0	35	28	24		
C _{in}	Maximum Input Capacitance		-	10	10	10	pF	
C _{out}	Maximum Output Capacitance		-	15	15	15	pF	
C _{PD}	Power Dissipation Capacitance (Note 2)		_	140	140	140	pF	

^{2.} C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: I_{CC} (operating) $\approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where N_{SW} = total number of outputs switching and f_{IN} = switching frequency.

AC WAVEFORMS

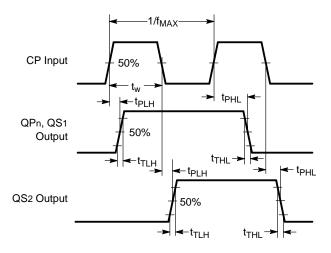
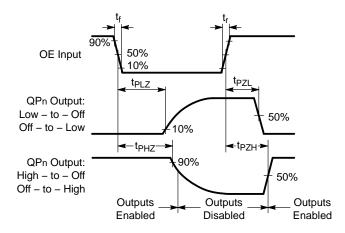
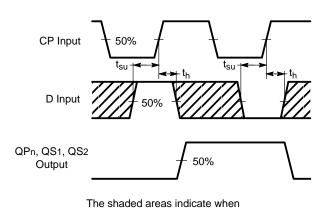


Figure 7. Waveforms showing the clock (CP) to output (QPn, QS1, QS2) propagation delays, the clock pulse width and the maximum clock frequency.

Figure 8. Waveforms showing the strobe (STR) to output (QPn) propagation delays, the strobe pulse width, the clock set-up and hold times for the strobe input.



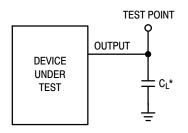


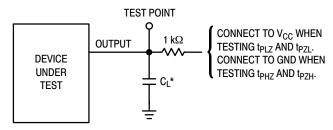
the input is permitted to change for predictable output performance.

Figure 9. Waveforms showing the 3-state enable and disable times for input OE.

Figure 10. Waveforms showing the data set-up and hold times for the data input.

TEST CIRCUITS





*Includes all probe and jig capacitance

Figure 11. AC Characteristics Load Circuits

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC4094ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4094ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC74HC4094ADTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74HC4094ADTR2G	TSSOP-16 (Pb-Free)	2500 / Tape & Reel
NLVHC4094BDTR2G*	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}Includes all probe and jig capacitance

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE



DATE 29 DEC 2006

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- THE NOTION AND TOLETANOING FER ANSI'Y 14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- PHOI HUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

 DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION

 SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D

 DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:			
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE	#1	
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1		
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2		
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2		
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3		
6.	BASE	6.	NO CONNECTION		BASE, #2	6.	COLLECTOR, #3		
7.	COLLECTOR	7.	ANODE	7.		7.	COLLECTOR, #4		
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4		
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4		
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4		
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3		
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3		
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2	OOL DEDING	COOTDONT
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2	SOLDERING	FOOTPRINT
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1		8X
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1		i.40 — →
								- 0	.40
STYLE 5:		STYLE 6:		STYLE 7:					16X 1.12
PIN 1.	DRAIN, DYE #1		CATHODE	PIN 1.	SOURCE N-CH				10% 1.12
2.	DRAIN, #1		CATHODE	2.	COMMON DRAIN (OUTPU	Τ\		1	16
3.	DRAIN, #2	3.		3.	COMMON DRAIN (OUTPU			, L	'0
3. 4.	DRAIN, #2	3. 4.	CATHODE	3. 4.	GATE P-CH	1)		- —	
4. 5.	DRAIN, #2	4. 5.	CATHODE	4. 5.	COMMON DRAIN (OUTPU	Τ\		, , , , , , , , , , , , , , , , , , , 	
5. 6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPU		16	5X 1 -	
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPU		0.5	58	, L
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH	•,			
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH				
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPU	T)			
11.	GATE, #3	11.		11.	COMMON DRAIN (OUTPU				
12.	SOURCE, #3	12.		12.	COMMON DRAIN (OUTPU				
13.	GATE, #2	13.		13.	GATE N-CH	.,			
14.	SOURCE, #2	14.		14.	COMMON DRAIN (OUTPU	T)			V PITCH
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPU				1 <u>+=</u> 1- 1
16.	SOURCE, #1		ANODE	16.	SOURCE N-CH	.,			
								□ 8	9 + - + -
									~
									' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '
									DIMENSIONS: MILLIMETERS

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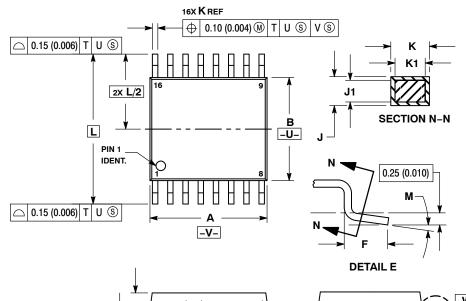
-T- SEATING PLANE





TSSOP-16 CASE 948F-01 ISSUE B

DATE 19 OCT 2006



NOTES

- JIES:
 DIMENSIONING AND TOLERANCING PER
 ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD
 FLASH. PROTRUSIONS OR GATE BURRS.
 MOLD EL ROLL OF GATE BURDS SUAL NO.
- MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
C		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.18	0.28	0.007	0.011	
7	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
Ы	6.40 BSC		0.252 BSC		
М	0 °	8 °	0 °	8 °	

SOLDERING FOOTPRINT

G



GENERIC MARKING DIAGRAM*

168888888 XXXX XXXX **ALYW** 188888888

XXXX = Specific Device Code Α = Assembly Location

= Wafer Lot L Υ = Year W = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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