



N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)			
30	0.0195 at V _{GS} = 10 V	8	9.2 nC			
30	0.023 at V _{GS} = 4.5 V	8	9.2110			

FEATURES

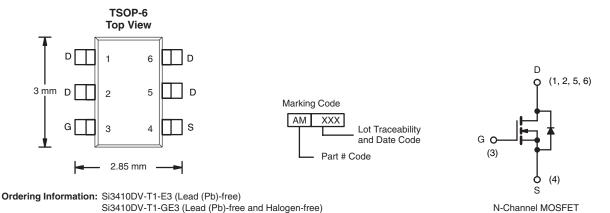
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

Pb-free RoHS COMPLIANT HALOGEN

FREE

APPLICATIONS

- · Notebook Load Switch
- Low Current dc-to-dc



Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 20	V	
	T _C = 25 °C		8 ^a	
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	1 , [8 ^a	
Continuous Diam Current (1) = 150 °C)	T _A = 25 °C	l lD	7.5 ^{b,c}	
	T _A = 70 °C		5.9 ^{b,c}	Α
Pulsed Drain Current	I _{DM} 3	30		
Continuous Course Drain Diada Current	T _C = 25 °C		2.7	
Continuous Source-Drain Diode Current	T _A = 25 °C	ls –	1.7 ^{b,c}	
	T _C = 25 °C		4.1	
Maximum Dawar Dissination	T _C = 70 °C		2.6	w
Maximum Power Dissipation	T _A = 25 °C	P _D	2 ^{b,c}	VV
	T _A = 70 °C		1.25 ^{b,c}	
Operating Junction and Storage Temperature Rang	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R _{thJA}	45	62.5	°C/W	
Maximum Junction-to-Foot	Steady State	R _{thJF}	25	30	G/ VV	

Notes

- a. Package Limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s
- d. Maximum under Steady State conditions is 110 $^{\circ}\text{C/W}.$

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V		
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		33		mV/°C		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	1 _D = 250 μΑ		- 6.2				
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1		3	V		
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA		
Zoro Cata Valtaga Drain Current	l	V _{DS} = 30 V, V _{GS} = 0 V			1	μΑ		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α		
	В	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.016	0.0195	Ω		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$		0.019	0.023			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 5 A		24		S		
Dynamic ^b								
Input Capacitance	C _{iss}			1295		pF		
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		170				
Reverse Transfer Capacitance	C _{rss}			72				
Tatal Oata Obarra	Q _g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		21.8	33	nC		
Total Gate Charge				9.2	14			
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 5 \text{ A}$		3.8				
Gate-Drain Charge	Q_{gd}			2.5				
Gate Resistance	R_{g}	f = 1 MHz		2.4		Ω		
Turn-On Delay Time	t _{d(on)}			21	40			
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		14	25			
Turn-Off DelayTime	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		20	40			
Fall Time	ì,			9	18			
Turn-On Delay Time	t _{d(on)}			10	20	ns		
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		8	16	-		
Turn-Off DelayTime	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		21	35			
Fall Time	ì,	-		8	16			
Drain-Source Body Diode Characteris	tics							
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			2.7			
Pulse Diode Forward Current	I _{SM}				30	A		
Body Diode Voltage	V _{SD}	$I_S = 1.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.77	1.2	V		
Body Diode Reverse Recovery Time	t _{rr}			21	40	ns		
Body Diode Reverse Recovery Charge	Q _{rr}	L 2 A dl/dt 100 A/va T 25 °C		15	30	nC		
Reverse Recovery Fall Time	t _a	$I_F = 3 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		13				
Reverse Recovery Rise Time	t _b			8		ns		

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

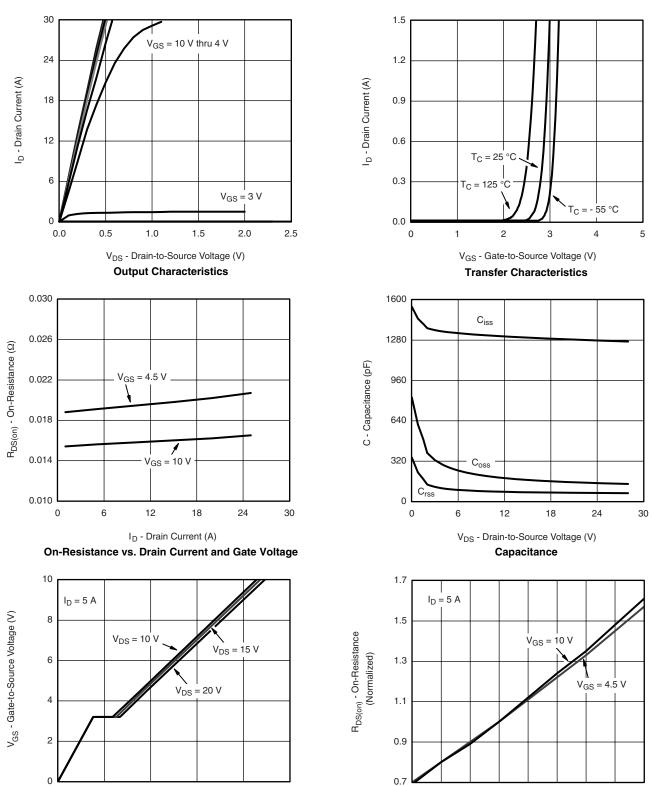
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

b. Guaranteed by design, not subject to production testing.





TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



10

Q_g - Total Gate Charge (nC)

Gate Charge

15

25

- 25

- 50

25

50

T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

75

125

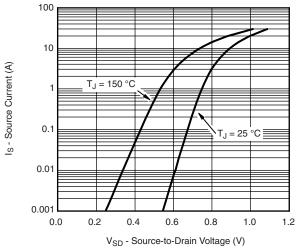
100

150

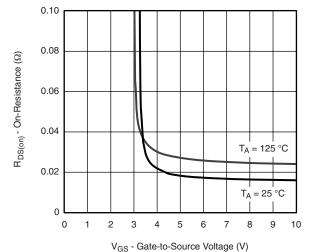
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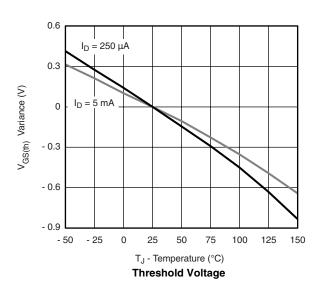
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

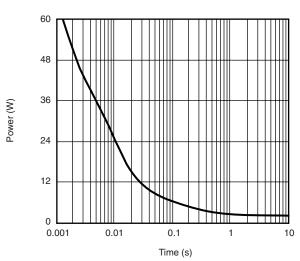


Source-Drain Diode Forward Voltage

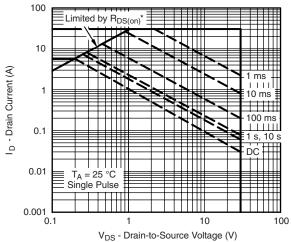


On-Resistance vs. Gate-to-Source Temperature





Single Pulse Power, Junction-to-Ambient

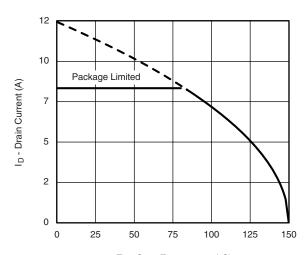


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

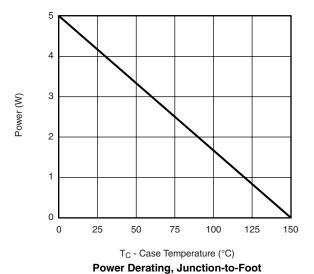


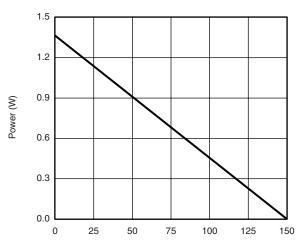
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$ - Case Temperature (°C)

Current Derating*





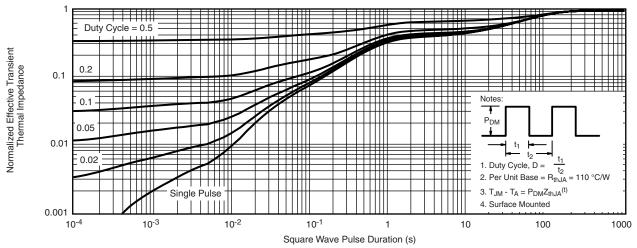
 T_A - Ambient Temperature (°C) $\label{eq:continuous} \mbox{Power Derating, Junction-to-Ambient}$

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

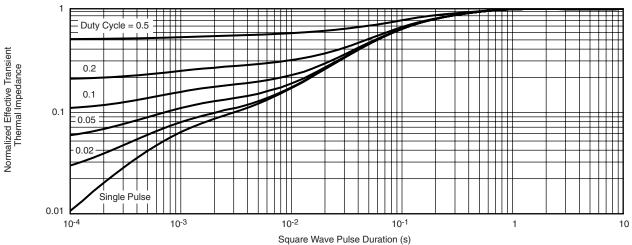
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69254.





TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C





5-LEAD TSOP







	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.008		
D	2.95	3.05	3.10	0.116 0.120		0.122	
E	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC		0.0374 BSC			
e ₁	1.80	1.90	2.00	0.071	0.079		
L	0.32	-	0.50	0.012	-	0.020	
L ₁	0.60 Ref			0.024 Ref			
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ1	7° Nom			7° Nom			
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540							

Document Number: 71200 18-Dec-06



Recommended Land Pattern For TSOP-5L / TSOP-6L



Note

• All dimensions are in inches (millimeter)

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