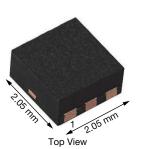


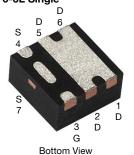
www.vishay.com

Vishay Siliconix

Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PowerPAK® SC-70-6L Single





Marking Code: QCXXXX

PRODUCT SUMMARY								
V _{DS} (V)	30							
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.065							
$R_{DS(on)}(\Omega)$ at $V_{GS} = 2.5 \text{ V}$	0.095							
I _D (A)	2.25							
Configuration	Single							
Package	PowerPAK SC-70							

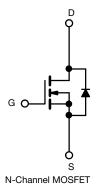
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % Rg and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	30	V		
Gate-source voltage		V_{GS}	± 12	V		
Continuous drain current a	T _C = 25 °C		2.25			
Continuous drain current 4	T _C = 125 °C	I _D	2.25			
Continuous source current (diode conduct	ion) ^a	I _S	2.25	Α		
Pulsed drain current ^a		I _{DM}	9			
Single pulse avalanche current	1 04	I _{AS}	9			
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	4	mJ		
Maximum payor dissination h	T _C = 25 °C	D	13.6	W		
Maximum power dissipation ^b	T _C = 125 °C	P_{D}	4.5			
Operating junction and storage temperatu	re range	T _J , T _{stg}	-55 to +175	00		
Soldering recommendations (peak temper	ature) ^{e, f}	-	260	°C		

THERMAL RESISTANCE RATINGS									
PARAMETER		SYMBOL	LIMIT	UNIT					
Junction-to-ambient	PCB mount c	R_{thJA}	90	°C/W					
Junction-to-case (drain)		R_{thJC}	11	C/VV					

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. Parametric verification ongoing

S17-0424-Rev. A, 03-Apr-17

- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					L			
Drain-source breakdown voltage	V_{DS}	V _{GS} =	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$			-	V	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	0.45	0.6	1.1	V	
Gate-source leakage	I _{GSS}	V _{DS} =	= 0 V, V _{GS} = ± 8 V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 30 V	-	-	1		
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 30 V, T _J = 125 °C	-	-	50	μΑ	
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 175 °C	-	-	250	7	
On-state drain current ^a	I _{D(on)}	V _{GS} = 4.5 V	$V_{DS} \ge 5 V$	10	-	-	Α	
		V _{GS} = 4.5 V	I _D = 3 A	-	0.038	0.065		
Dunius annuas au atata unaintaura 3	Б	V _{GS} = 4.5 V	I _D = 3 A, T _J = 125 °C	-	-	0.077	Ω	
Drain-source on-state resistance a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 3 A, T _J = 175 °C	-	-	0.090		
		V _{GS} = 2.5 V	I _D = 3 A	- 0.048 0.		0.095	7	
Forward transconductance b	9fs	V _{DS}	V _{DS} = 15 V, I _D = 2 A			-	S	
Dynamic ^b								
Input capacitance	C _{iss}			=	312	440	pF	
Output capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 20 \text{ V}, f = 1 \text{ MHz}$	-	56	80		
Reverse transfer capacitance	C _{rss}	1		-	29	41		
Total gate charge ^c	Qg				4.6	6		
Gate-source charge ^c	Q _{gs}	V _{GS} = 4.5 V	$V_{DS} = 15 \text{ V}, I_D = 4.2 \text{ A}$	-	0.65	-	nC	
Gate-drain charge ^c	Q _{gd}	1		-	0.9	-		
Gate resistance	R _g		2.1	3.6	5.7	Ω		
Turn-on delay time ^c	t _{d(on)}			-	7.3	11		
Rise time ^c	t _r	$V_{DD} = 10 \text{ V}, R_{L} = 10 \Omega$		-	18	26	ns	
Turn-off delay time c	t _{d(off)}	I _D ≅ 1 A, \	-	21	32			
Fall time ^c	t _f	1		-	9.5	14		
Source-Drain Diode Ratings and Char	acteristics ^b							
Pulsed current ^a	I _{SM}			-	-	24	Α	
Forward voltage	V _{SD}	I _F =	=.	0.75	1.2	V		

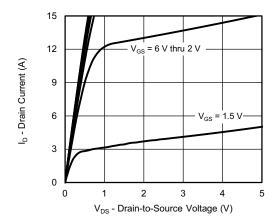
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

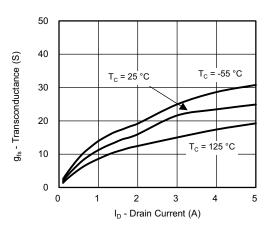
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



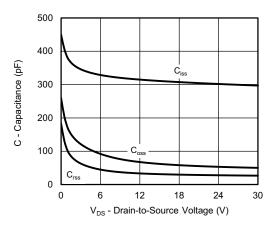
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



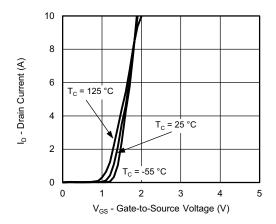
Output Characteristics



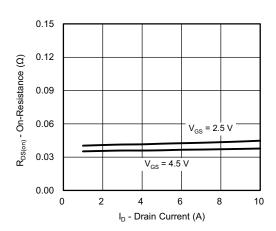
Transconductance



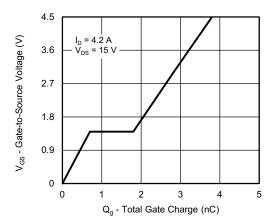
Capacitance



Transfer Characteristics



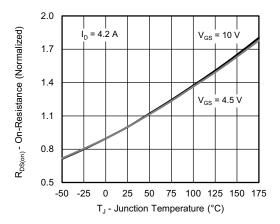
On-Resistance vs. Drain Current



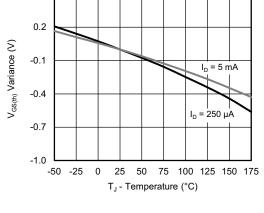
Gate Charge



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

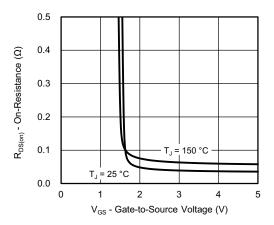


On-Resistance vs. Junction Temperature

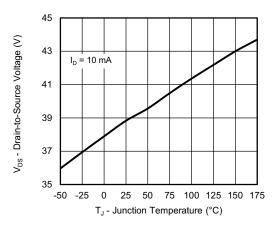


0.5

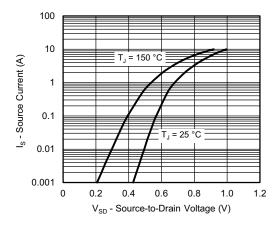
Threshold Voltage



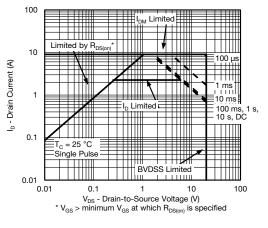
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



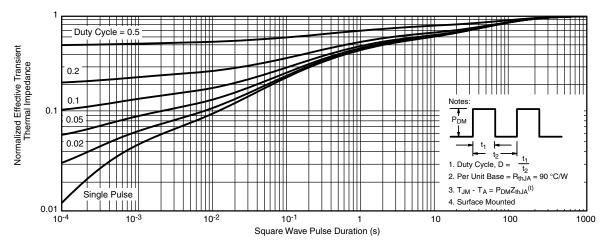
Source Drain Diode Forward Voltage



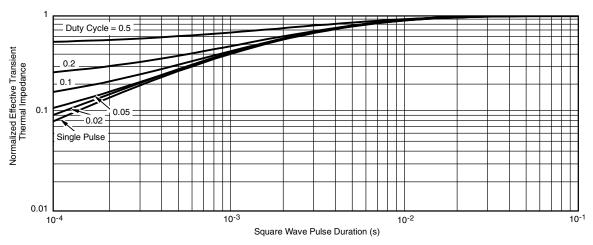
Safe Operating Area



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

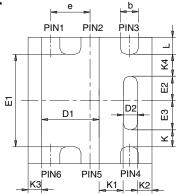
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75522.

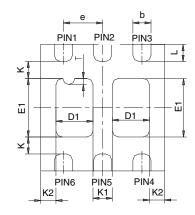




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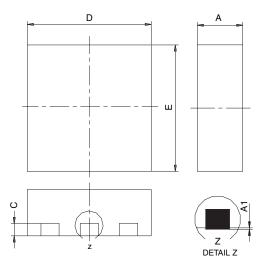
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

		SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	,	0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP		0.275 TYP			0.011 TYP			
K1		0.400 TYP 0.016 TYP				0.320 TYP			0.013 TYP				
K2		0.240 TYP	1	0.009 TYP			0.252 TYP			0.010 TYP			
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP 0.014 TYP											
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
ECNI- C C	7404 D	. 0 00 1	. 07										

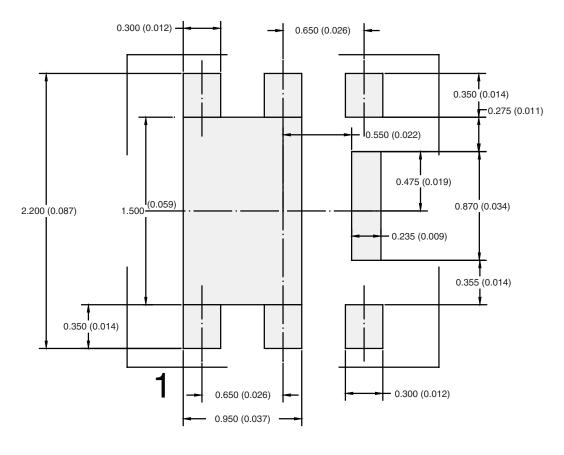
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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