AN-1494

## Converting a Single-Ended Signal with the AD7982 Differential PuISAR ADC

## CIRCUIT FUNCTION AND BENEFITS

There are many applications that require a single-ended analog signal, either bipolar or unipolar, to be converted by a high resolution, differential input analog-to-digital converter (ADC). This dc-coupled circuit converts a single-ended input signal to a differential signal suitable for driving the AD7982, an 18-bit, 1 MSPS member of the PulSAR ${ }^{\circ}$ family of ADCs.

This circuit uses the ADA4941-1 single-ended to differential driver and the ADR435 ultralow noise 5.0 V voltage reference. The circuit can accept many types of single-ended input signals, including bipolar or unipolar, ranging from high voltage to low voltage. Direct coupling is maintained throughout. If board space is at a premium, all the integrated circuits (ICs) shown in Figure 1 come in small packages; either a $3 \mathrm{~mm} \times 3 \mathrm{~mm}$ leadframe chip scale package (LFCSP) or a $3 \mathrm{~mm} \times 5 \mathrm{~mm}$ micro small outline package (MSOP).


Figure 1. Single-Ended to Differential DC-Coupled Driver Circuit (Simplified Schematic)

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11/2017—Rev. A to Rev. B
Document Title Changed from CN0032 to AN-1494... ..... Universal
Changes to Figure 1 .....  1
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7/2009—Rev. 0 to Rev. AUpdated Format
$\qquad$ Universal
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## CIRCUIT DESCRIPTION

The differential input voltage range of the AD7982 is set by the voltage on the REF pin. For $V_{\text {Ref }}=5 \mathrm{~V}$, the differential input voltage range is $\pm \mathrm{V}_{\text {REF }}= \pm 5 \mathrm{~V}$. The voltage gain (or attenuation) from the single-ended source, $\mathrm{V}_{\text {IN }}$, to the OUT+ pin of the ADA4941-1 is set by the ratio of R2 to R1. The ratio of Resistor R2 to Resistor R1 is equal to the ratio of $\mathrm{V}_{\text {REF }}$ to the peak-to-peak input voltage at $\mathrm{V}_{\text {IN }}$. For a peak-to-peak, singleended input voltage of 10 V and $\mathrm{V}_{\text {ref }}=5 \mathrm{~V}$, the ratio of Resistor R2 to Resistor R1 is 0.5 . The signal at the OUT+ pin is inverted (gain $=-1$ ) by the upper half of the ADA4941-1, which supplies the opposite phase output signal at the OUT- pin. The absolute value of Resistor R1 determines the input impedance of the circuit. Feedback capacitor $C_{F}$ is chosen based on the desired signal bandwidth, which is approximately $1 /\left(2 \pi \mathrm{R}_{2} \mathrm{C}_{\mathrm{F}}\right)$. The $20 \Omega$ resistors and the 2.7 nF capacitors act as a 3 MHz , single-pole, low-pass noise filter.
Resistors R3 and R4 set the common-mode voltage on the INinput of the AD7982. The value of this common-mode voltage is $V_{\text {offset }} \times(1+\mathrm{R} 2 / \mathrm{R} 1)$, where $\mathrm{V}_{\text {offset } 2}=\mathrm{V}_{\text {ref }} \times \mathrm{R} 3 /(\mathrm{R} 3+\mathrm{R} 4)$. Resistors R5 and R6 set the common-mode voltage on the IN+ input of the ADC. This voltage is equal to $V_{\text {offsetil }}=\mathrm{V}_{\text {ref }} \times \mathrm{R} 5 \div$ ( $\mathrm{R} 5+\mathrm{R} 6$ ). The common-mode voltage of the ADC, which is equal to $\mathrm{V}_{\text {offsefti, }}$, should be close to $\mathrm{V}_{\text {ref }} / 2$. This implies that R5 = R6. Table 1 shows some possible standard $1 \%$ values for the resistors for popular input voltage ranges.
The ADA4941-1 operates on supply voltages of 7 V and -2 V . Because each output must swing from 0 V to 5 V , the positive supply voltage must be a few hundred millivolts greater than 5 V and the negative supply must be a few hundred millivolts more negative than 0 V . For this circuit, supply voltages of 7 V and -2 V are chosen. The 7 V supply also provides sufficient
headroom to power the ADR435. Other voltages are possible, provided the absolute maximum total supply voltage on the ADA4941-1 does not exceed 12 V and the headroom requirement of the ADR435 is observed.
The AD7982 requires a 2.5 V supply for $\mathrm{V}_{\mathrm{DD}}$ as well as a $\mathrm{V}_{\mathrm{IO}}$ supply (not shown in Figure 1), which can range between 1.8 V and 5 V , depending upon the input/output logic interface levels.
This circuit is not sensitive to power supply sequencing. The AD7982 inputs can withstand up to $\pm 130 \mathrm{~mA}$ maximum during momentary overvoltage conditions.
The AD7982 serial peripheral interface (SPI)-compatible serial interface (not shown in Figure 1) has the ability to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator using the SDI input pin. It is compatible with $1.8 \mathrm{~V}, 2.5 \mathrm{~V}, 3 \mathrm{~V}$, and 5 V logic, using the separate $\mathrm{V}_{\mathrm{IO}}$ supply. For full details on the SPI interface, digital modes, and logic power options, see the AD7982 data sheet.
Excellent layout, grounding, and decoupling techniques must be utilized to achieve the desired performance from the circuits discussed in this note. As a minimum, use a 4-layer printed circuit board (PCB) with one ground plane layer, one power plane layer, and two signal layers.

All IC power pins must be decoupled to the ground plane with low inductance, multilayer ceramic capacitors (MLCC) of $0.01 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$ (this is not shown in Figure 1 for simplicity). Follow the recommendations on the individual data sheets for the ICs referenced in the References section.

Consult the EVAL-FDA-1 and EVAL-AD7982 evaluation board user guides for the recommended layout and critical component placement of each product.

Table 1. Circuit Values and Voltages for Popular Input Voltage Ranges

| $\mathbf{V I N}_{\text {IN }}(\mathbf{V})$ | $\mathrm{V}_{\text {offseti }}(\mathrm{V})$ | $\mathrm{V}_{\text {offset2 }}(\mathrm{V})$ | OUT+ (V) | OUT- (V) | R1 (k) | R2 (k) | R4(k) | R3, R5, R6 (kת) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| +20, -20 | 2.5 | 2.203 | -0.01, +4.96 | 5.0, 0.04 | 8.06 | 1.00 | 12.70 | 10.00 |
| +10, -10 | 2.5 | 2.000 | 0.01, 4.99 | 4.99, 0.01 | 4.02 | 1.00 | 15.0 | 10.00 |
| +5, -5 | 2.5 | 1.667 | 0.00, 5.00 | 5.00, 0.00 | 2.00 | 1.00 | 20.0 | 10.00 |

## COMMON VARIATIONS

For different reference voltages, the ADR430, ADR431, ADR433, ADR434, and ADR435 family of references has a wide range of values that can interface with the ADC.

## REFERENCES

Kester, Walt. 2005. Chapter 6 and Chapter 7. The Data Conversion Handbook. Analog Devices, Inc.

Kester, Walt. 2006. High Speed System Applications. Chapter 2, "Optimizing Data Converter Interfaces." Analog Devices.
MT-031 Tutorial, Grounding Data Converters and Solving the Mystery of "AGND" and "DGND". Analog Devices.

MT-035 Tutorial, Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues. Analog Devices.
MT-074 Tutorial, Differential Drivers for Precision ADCs. Analog Devices.
MT-101 Tutorial, Decoupling Techniques. Analog Devices.
Voltage Reference Wizard Design Tool.

