

N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
12	0.0055 at V _{GS} = 4.5 V	17			
	0.008 at V _{GS} = 2.5 V	14			

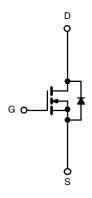
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFETs
- PWM Optimized for High Efficiency
- Low Output Voltage
- 100 % R_q Tested

ROHS COMPLIANT HALOGEN FREE Available

APPLICATIONS

- Synchronous Rectifier
- · Point-of-Load Synchronous Buck Converter



N-Channel MOSFET

	SO-8		
S 1	_	8	D
S 2	1	7	D
S 3	1	6	D
G 4	1	5	D
	Top View	ļ	

Ordering Information: Si4866DY-T1-E3 (Lead Pb)-free)

Si4866DY-T1-GE3 (Lead Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	$T_A = 25$ °C, unles	ss otherwise n	oted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	12		
Gate-Source Voltage		V _{GS}	± 8		V
0 11 0 1/T 150 00\3	T _A = 25 °C	I _D	17	11	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		14	8	
Pulsed Drain Current		I _{DM}	± 50		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.7	1.40	
	T _A = 25 °C	- P _D	3.0	1.6	W
Maximum Power Dissipation ^a	T _A = 70 °C		2.0	1.0	
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Manipular lunction to Ambient (MOCFET)	t ≤ 10 s	R_{thJA}	34	41	°C/W	
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		67	80		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	19		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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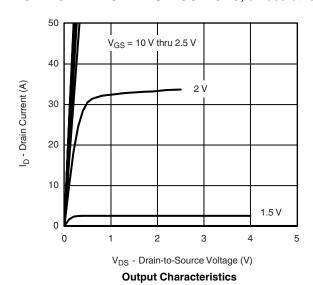
MOSFET SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.6			V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zava Cata Valtana Duain Comunit		V _{DS} = 9.6 V, V _{GS} = 0 V	1		1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 9.6 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			5	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	40			Α
D : 0	В	$V_{GS} = 4.5 \text{ V}, I_D = 17$,		0.0055	0
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 14$		0.0065	0.008	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 6 V, I _D = 17		80		S
Diode Forward Voltage ^a	V_{SD}	I _S = 2.7 A, V _{GS} = 0 V		0.70	1.1	V
Dynamic ^b						
Total Gate Charge	Q_g			21	30	
Gate-Source Charge	Q_{gs}	$V_{DS} = 6 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 17 \text{ A}$		4.6		nC
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_{G}		1.5	2.3	3.9	Ω
Turn-On Delay Time	t _{d(on)}			28	42	
Rise Time	t _r	V_{DD} = 6 V, R_L = 6 Ω		32	48	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong\text{1 A, V}_\text{GEN}=\text{4.5 V, R}_\text{G}=\text{6}~\Omega$		82	123	ns
Fall Time	t _f			35	53	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.7 A, dI/dt = 100 A/μs		60	90	

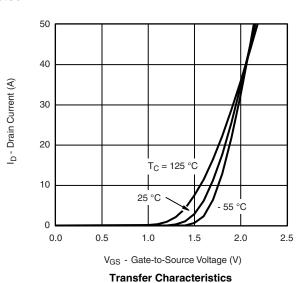
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

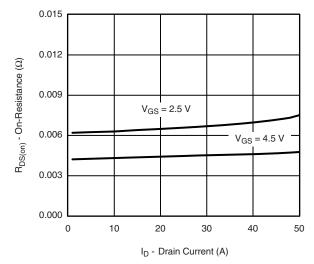




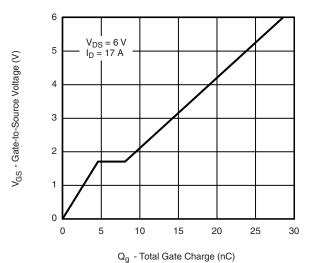


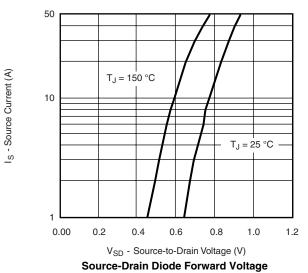


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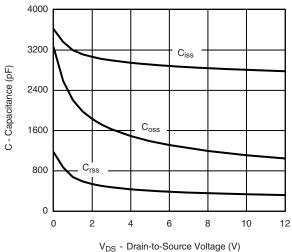


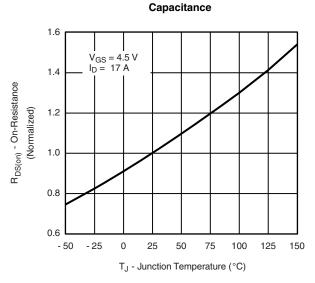
On-Resistance vs. Drain Current



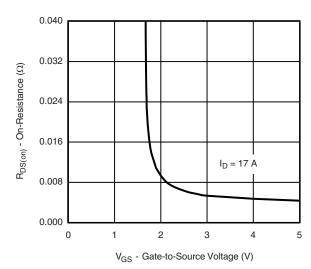


Gate Charge





On-Resistance vs. Junction Temperature

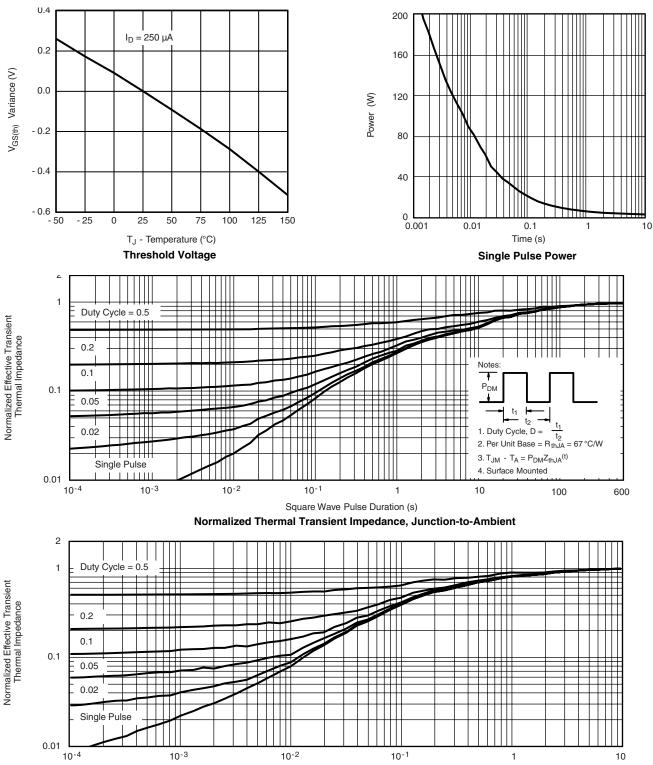


On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71699.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Bey 11-Sep-06						

DWG: 5498

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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